Notice of References Cited	Application/Control No. 09/823,929	Applicant(s)/Patent Under Reexamination ORCHARD, JOHN T.	
	Examiner Chat C. Do	Art Unit 2124	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,067,613	05-2000	Balmer, Keith	712/32
	B	US-5,796,644	08-1998	Jiang, Shao-Kun	708/501
	C	US-5,500,811	03-1996	Corry, Alan G.	708/319
	D	US-6,484,193	11-2002	Choe et al.	708/625
	E	US-6,535,901	03-2003	Grisamore, Robert T	708/629
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Marek et al., Minimization of multiple-valued input multi-output mixed-radix exclusive sums of products for incompletely specified boolean functions, 1989, IEEE, pages 256-263.
	V	Chu et al., A boolean function generator with learning capibility, 1991, IEEE, pages 845-856.
	W	Chang et al., Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs, Nov. 1999, IEEE Computers and Digital Techniques, pages 309-315.
	X	Fang et al., A hierarchical functional structuring and partitioning approach for multiple-FPGA implmentations, Oct. 1997, IEEE Computer-Aided Design of Integrated Circuits and Systems, pages 1188-1195.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.